# “Software-First” Approach in Emulation

Address TTM Requirements with a Production-Ready Silicon on Day 0

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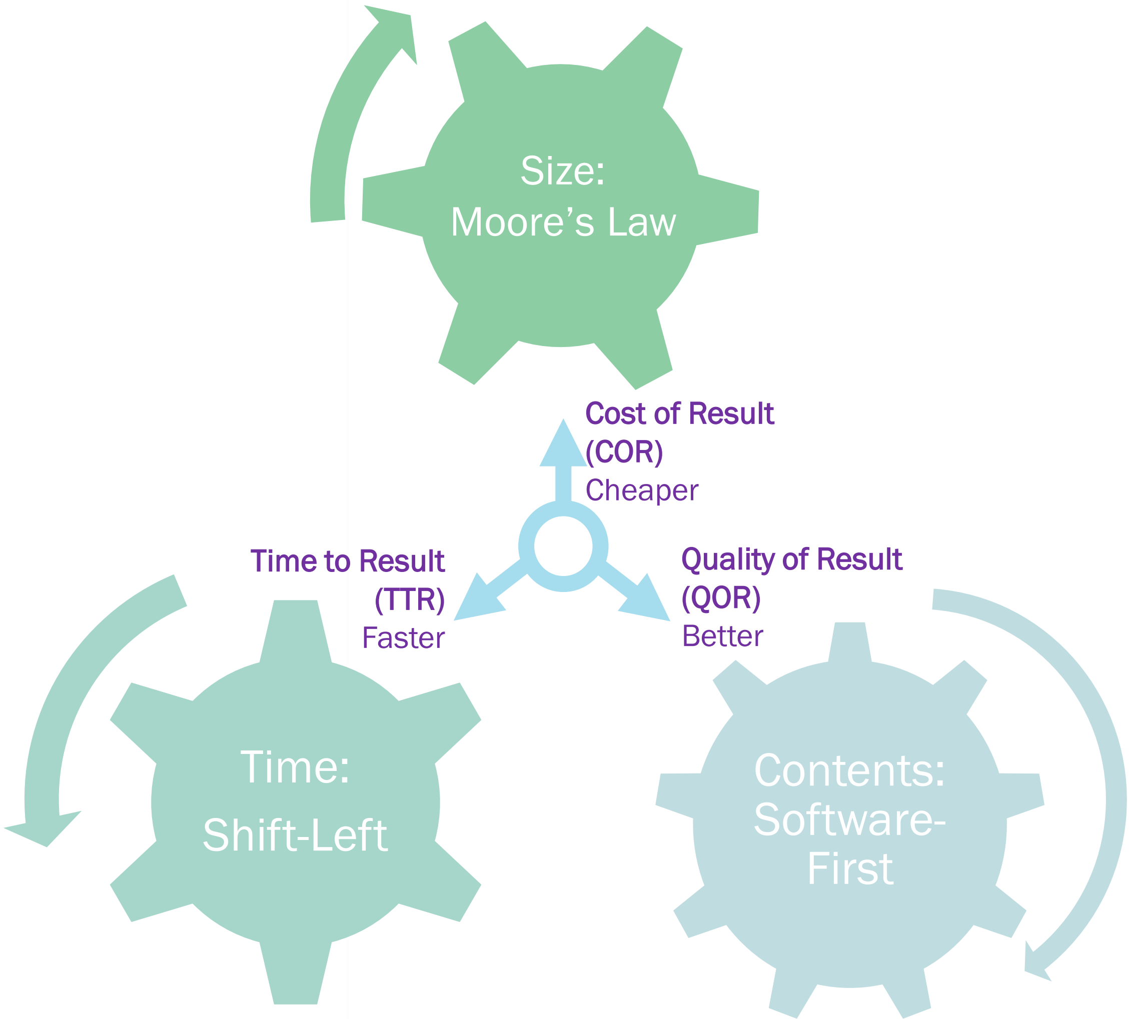
# Agenda

- Emergence of Verification Complexity
- User Requirements’ Correlation to EDA through HW and Use case Enabling
- Examples of Post-Si Content Enabling in Pre-Si Environment
- Summary with Industry Assessment

# Emergence of Verification Complexity




**Cost of Results**

What's my total cost of verification?

**Quality of Result**

Can I trust my env to run for multiple days/weeks?

Do I have a solution to support multi-Billion gate designs?

**Time to Result**

Can I enable post-Si workloads in pre-Si environment?

Can my testcase run faster?

# User Requirements for Hardware Assisted Verification

## Verification Use Cases

Early RTL verification
↓
RTL regression
↓
SW bring-up
↓
SW/HW validation
↓
Performance/Power
↓
Compliance/Certification

## Why HAV? (HW Assisted Verification)

**A Typical User Scenario for "software-first":**
SoC level testing using real world scenarios requires Trillion cycle execution on Billion gate designs

**Challenge w/ Simulation:**
Low simulation performance makes it a non-starter

**Industry Trend:**
HAV has become primary solution for DV sign-off

## User Requirements for "Software-first" approach

**Fastest:**
Test execution time

**Unmatched Reliability:**
Weeks of uninterrupted run

**Scalability:**
Support multi-Billion gates

**Software-first:**
Collaterals for SW bring-up

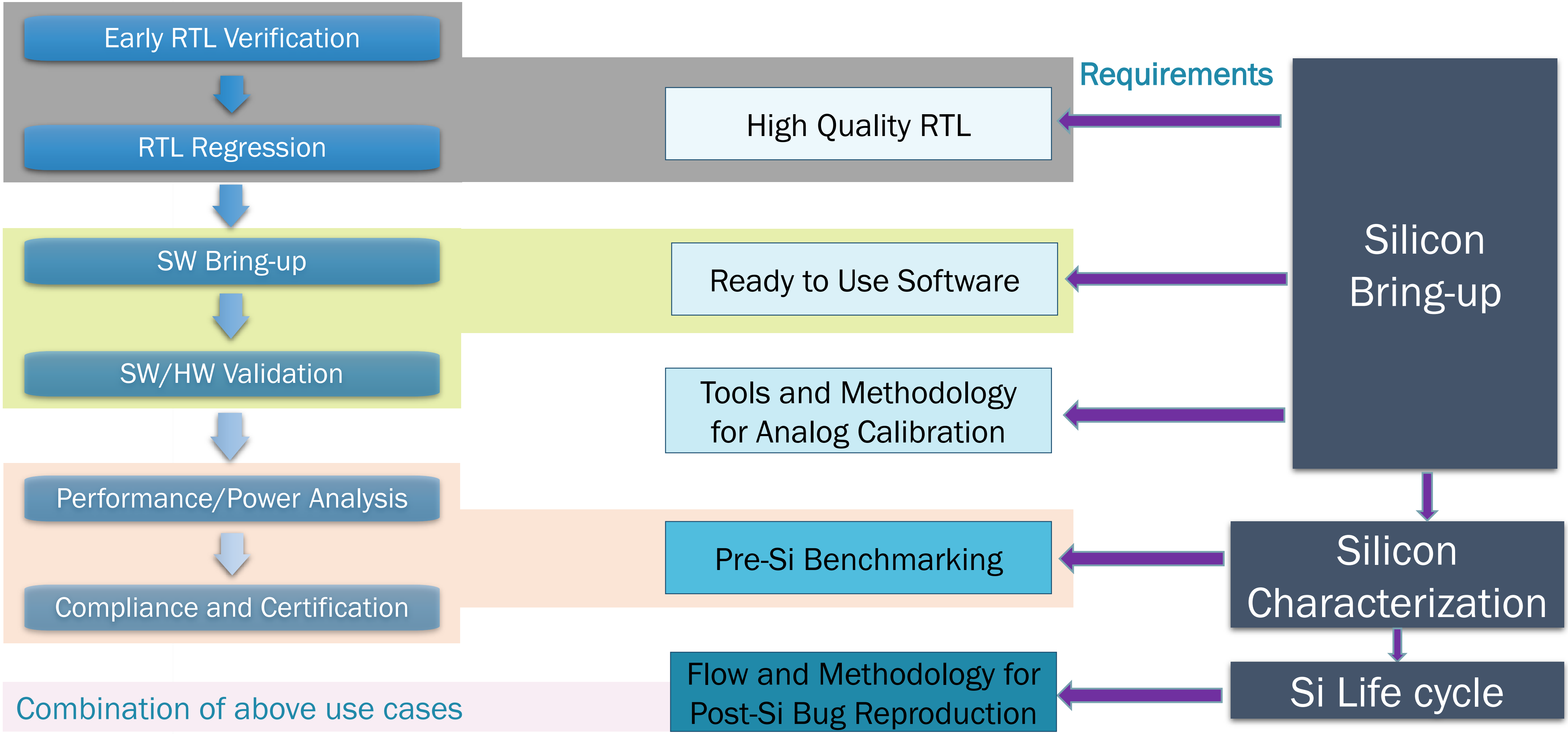
**Shift-left:**
Post-Si contents in Pre-Si

**Cost Effective:**
Offer best TCO


## Example of Industry Solution (ZeBu Server 5)

- Up to 8 MHz Perf
- 99.9% + uptime
- Up to 30BG capacity
- Hybrid, Real devices
- Power & Perf Analysis
  Compliance & Certification
- 3BG/$m^2$ Capacity density
  <6 kW/BG Power usage

# Verification Use Cases' Correlation w/ Si Readiness

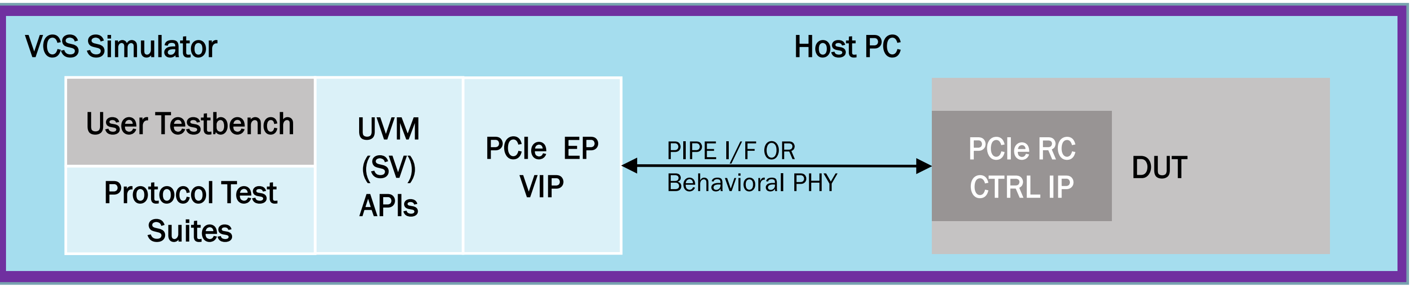


# Testbench Requirements for All Use Cases

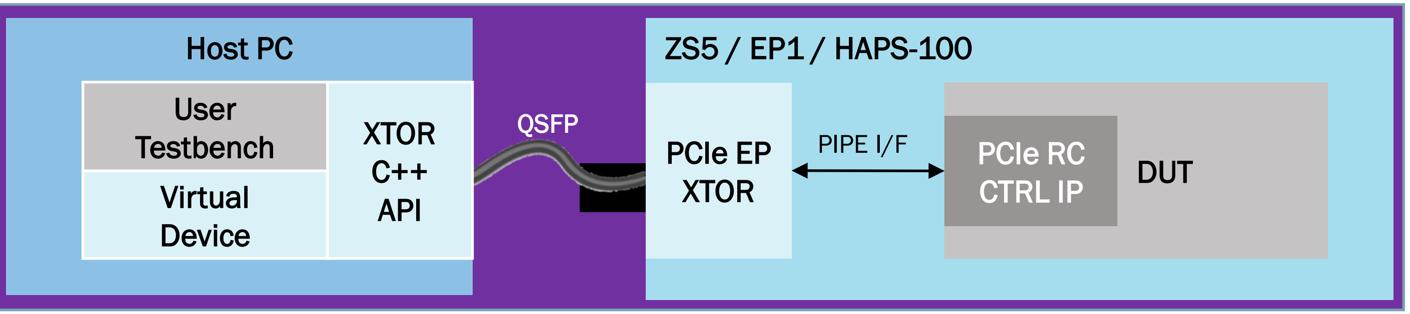
| | Verification IP | Transactors | Hybrid | Speed Adaptors | Physical Protocol I/Fs | IP Prototyping Kits |
|---|---|---|---|---|---|---|
| Early RTL Verification | ✓ | ✓ | | | | |
| RTL Regression | ✓ | ✓ | | | | |
| SW Bring-up | | ✓ | ✓ | ✓ | ✓ | ✓ |
| SW/HW Validation | | ✓ | ✓ | ✓ | ✓ | ✓ |
| Performance & Power Analysis | | ✓ | ✓ | ✓ | ✓ | ✓ |
| Compliance & Certification | | | ✓ | ✓ | ✓ | ✓ |

# Industry Solutions for Testbench Requirements

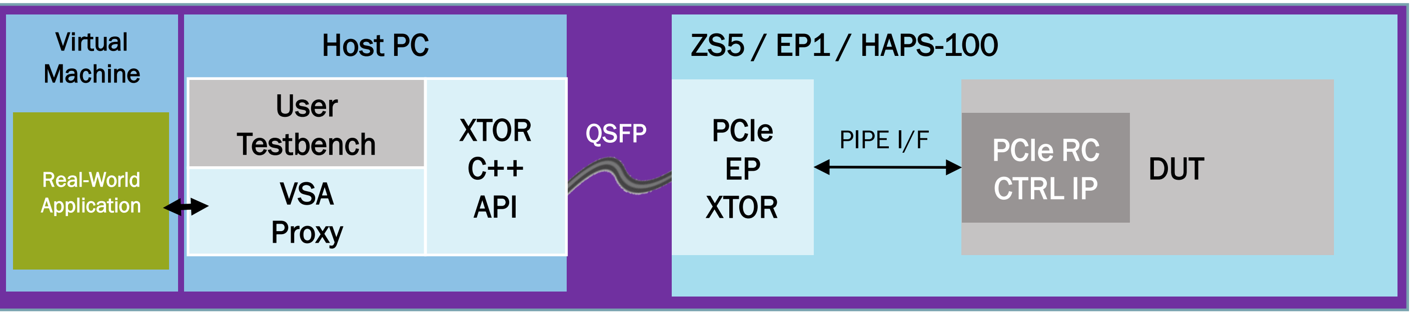
## Verification IP
- ✓ Early RTL verification
- ✓ RTL regressions




## Transactors
- ✓ RTL regressions
- ✓ SW Bring-up
- ✓ Performance/Power Analysis



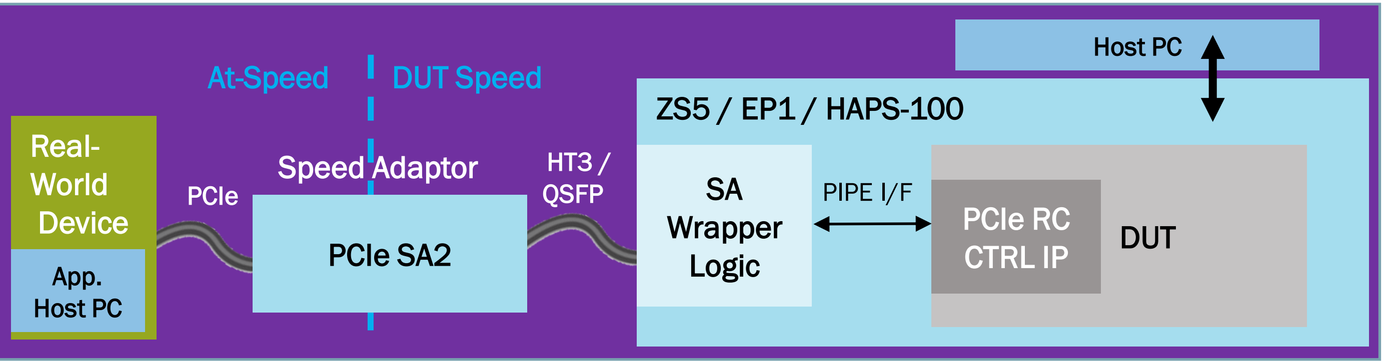

## Virtual Host Solutions
- ✓ SW Bring-up
- ✓ HW/SW Validation
- ✓ Performance/Power Analysis



# Industry Solutions for Testbench Requirements

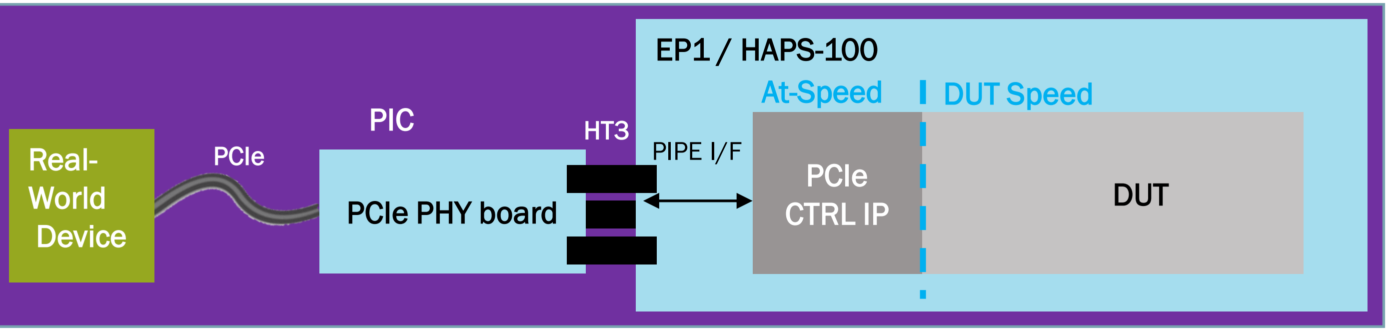
## Speed Adaptor (SA)

- ✓ SW Bring-up
- ✓ HW/SW Validation
- ✓ Performance/Power Analysis
- ✓ Compliance and Certification



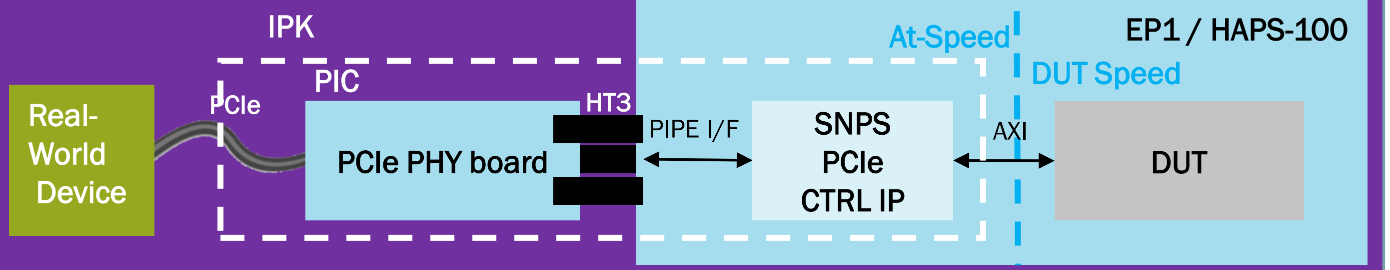

## Protocol Interface Card (PIC)

- ✓ SW Bring-up
- ✓ HW/SW Validation
- ✓ Compliance and Certification

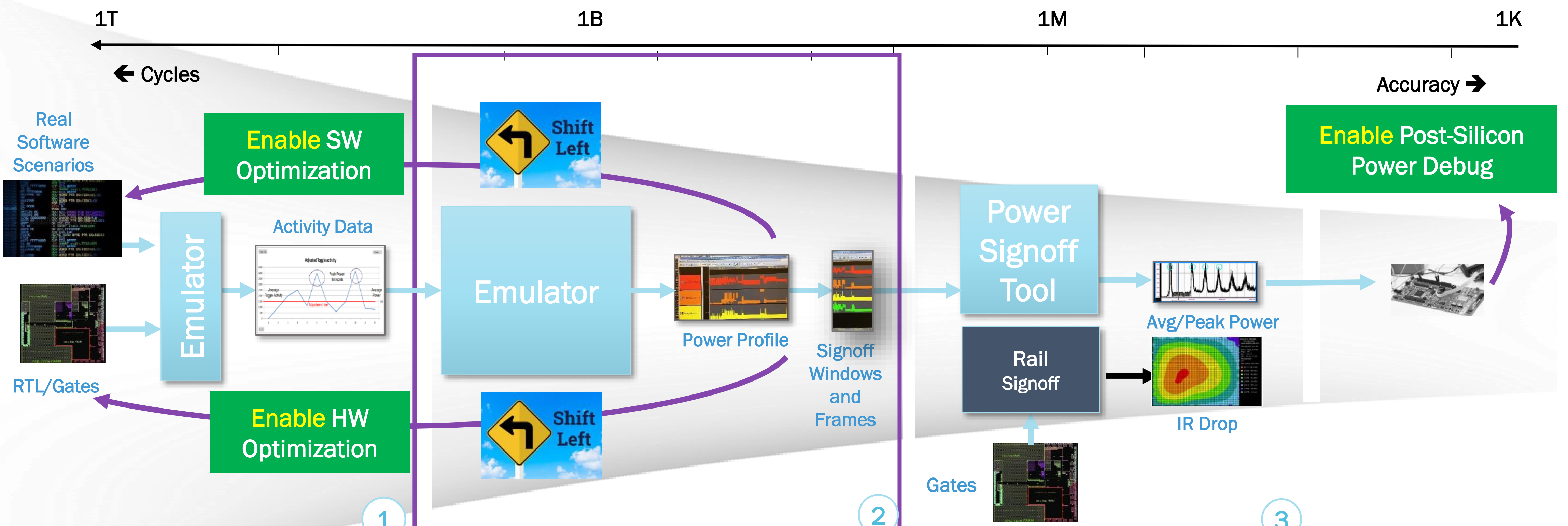



## IP Prototyping Kit (IPK)

- ✓ SW Bring-up
- ✓ HW/SW Validation
- ✓ Compliance and Certification



# SW-driven Power Estimation




1
**HAV: Emulation**
Activity data for the entire software workload

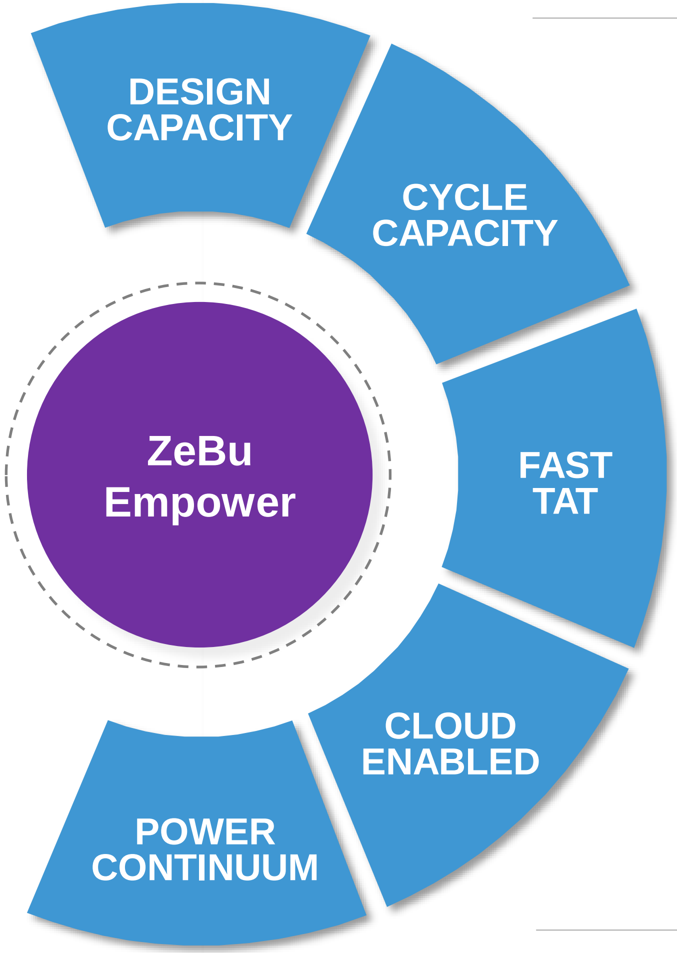
2
**High Performance Power Profiling for Software Workloads**
SW, HW power optimization with real workloads
Identify signoff windows and frames

3
**Power and Rail Signoff**
Highest accuracy power analysis
Static and dynamic IR drop

4
**Silicon Power Measurement**
Is power meeting spec/target?

User Requirements: HW,SW power optimization, post-silicon power debug, **and** power signoff with **real-world** scenarios

# Technology Requirements for Power Estimation




**DESIGN CAPACITY: Billion Gates**

- $2^{64}$ flattened design object capacity, binary save/restore
- 10x compaction for most designs, 100x for AI designs

**CYCLE CAPACITY: 100M cycles**

- Billion cycle Weighted Activity Profile (WAP)
- Cycle power for 100M cycles with actionable accuracy

**FAST TAT: Real Workload Processing in a Day**

- 300MG design, 1.5M cycles in 12hrs
- 5M cycles for GPU designs in 3hrs

**CLOUD ENABLED: Optimized Compute/Storage for Local Clouds**

- 46M cycles for GPU in 2.5hrs using 150 CPUs of 32GB local cloud
- Scalable to 2K+ CPU cores in low memory 32GB local cloud

**POWER CONTINUUM: Continuity from SW Use Case to Sign-Off**

- Reuse existing ZeBu models
- Feeding output into PrimePower (within 5% signoff accuracy)

# Shift-Left for Performance Analysis

## A case study of SSD controller device

### User Requirements

**System Setup**

- ❑ Support for different users: Verification team, SW developers
- ❑ Real world traffic, perf validation at high speed
- ❑ Support for multiple bus protocol and memory I/F

**Design Analysis**

- ❑ Count, latency and throughput analysis
- ❑ User friendly graphical analytics
- ❑ Synchronized view for protocol & perf analyzer

JTAG Debugger (DStream,Trace32,MDB)

TARMAC (Offline Verdi HW/SW Debug)


Speed Adaptor


PCIe/CXL/UFS
Virtual Host
(Windows/Linux)

SSD Controller DUT

DDR I/F

Processor (MCU)

Host I/F

Buffer Mgmt (Ramdisk)

Flash Controller

GPIO I/F

Flash Memory Model
OR
Flash Adaptor Card

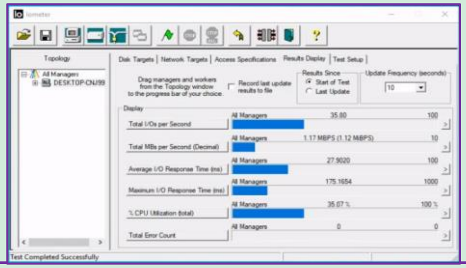
PCIe/NVMe/UFS Analyzer

DDR Model

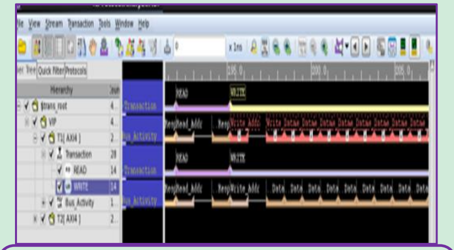
UART/I2C Model

AMBA Monitor

Flash Trace logger

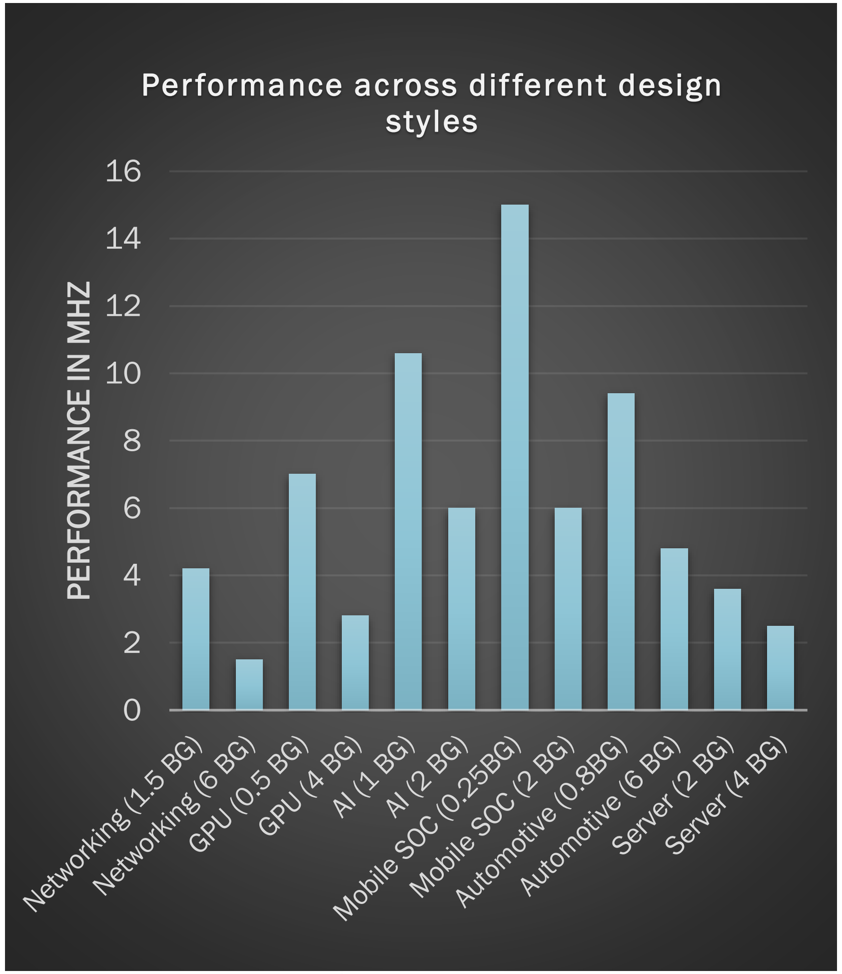

Real world traffic (IOMeter) / Compliance tests (FIO & UNH-IOL)


Platform Architect


Verdi Protocol Analyzer

# Summary: Industry Assessment

## Synopsys Emulation Delivers Shift-Left with Software-First Verification Approach




**Shift Left**

**Mobile SoC Provider:**
*Our designers can now identify SoC issues early in the design cycle and make our products more competitive in the market.*

**Software First**

**Leading Processor Company:**
*We booted BIOS successfully in 1.5 hrs on a large CPU RTL model. Before ZeBu EP1 we could only boot to that level using virtual/hybrid models.*

**High Perf**

**Mobile Compute Company:**
*The unparalleled performance will encourage us to hunt more aggressively for bugs. It has already exposed a firmware bug.*

**Reliability**

**CPU Provider:**
1 Trillion Software Cycles in <10 Days; 5 mins of real time boot and benchmark tests enabled in pre-Si env. operations. Full Windows

# Thank You